Cal Poly Pomona

2’s Compliment Addition to 7-Segment Display & Negative LED

Experiment 6

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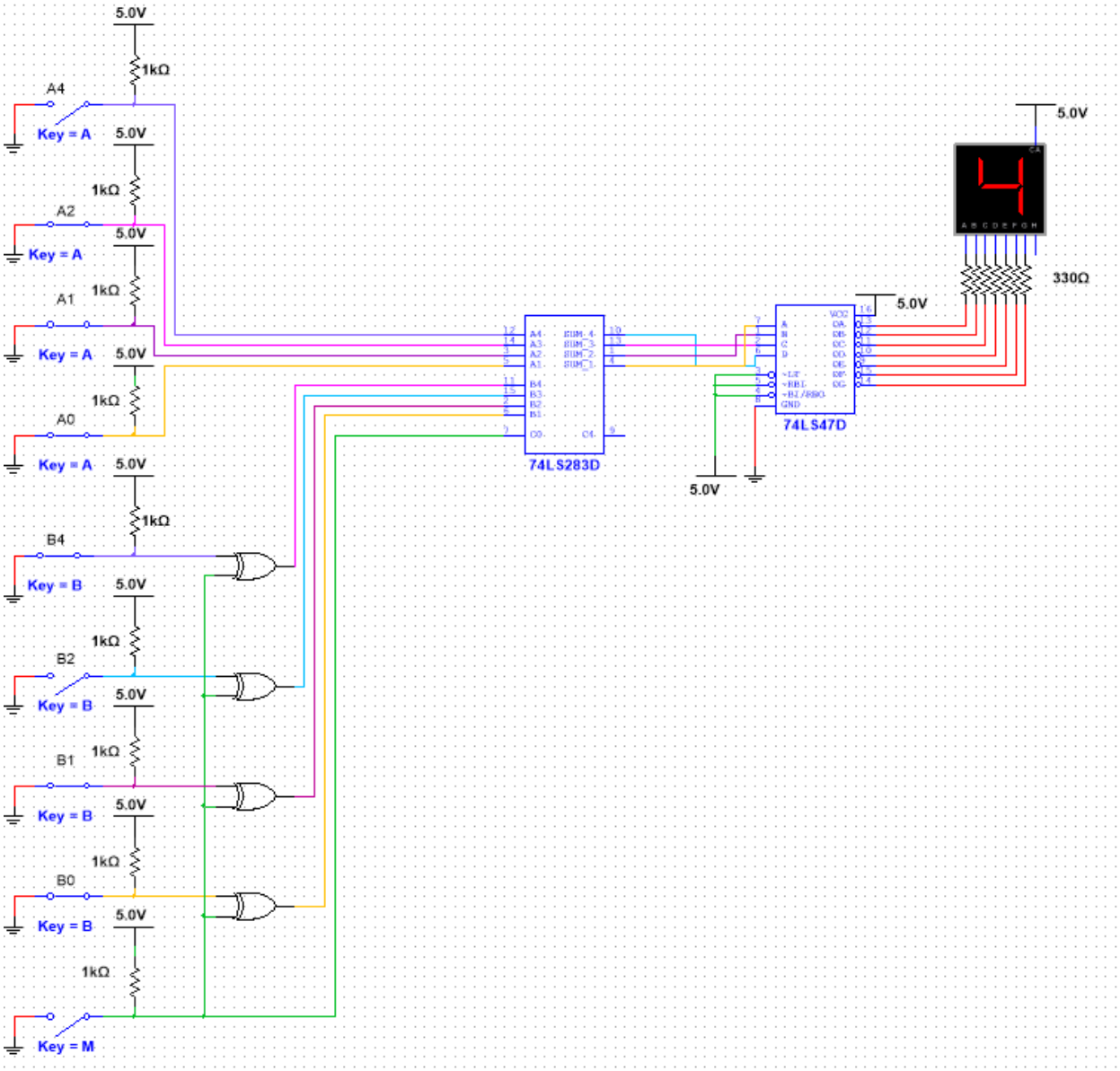
0.0 PRELAB

0.1 Design a 4-bit adder/subtractor using only full adders and EXCLUSIVE- OR gates. Do not use any multiplexers.

We designed a 4-bit adder/subtractor using one full adder and XOR gates. The XOR gates control whether B is inverted (for subtraction) depending on the mode select input **M**. When M=0, normal addition occurs; when M=1, subtraction (A + two's complement of B) is performed.

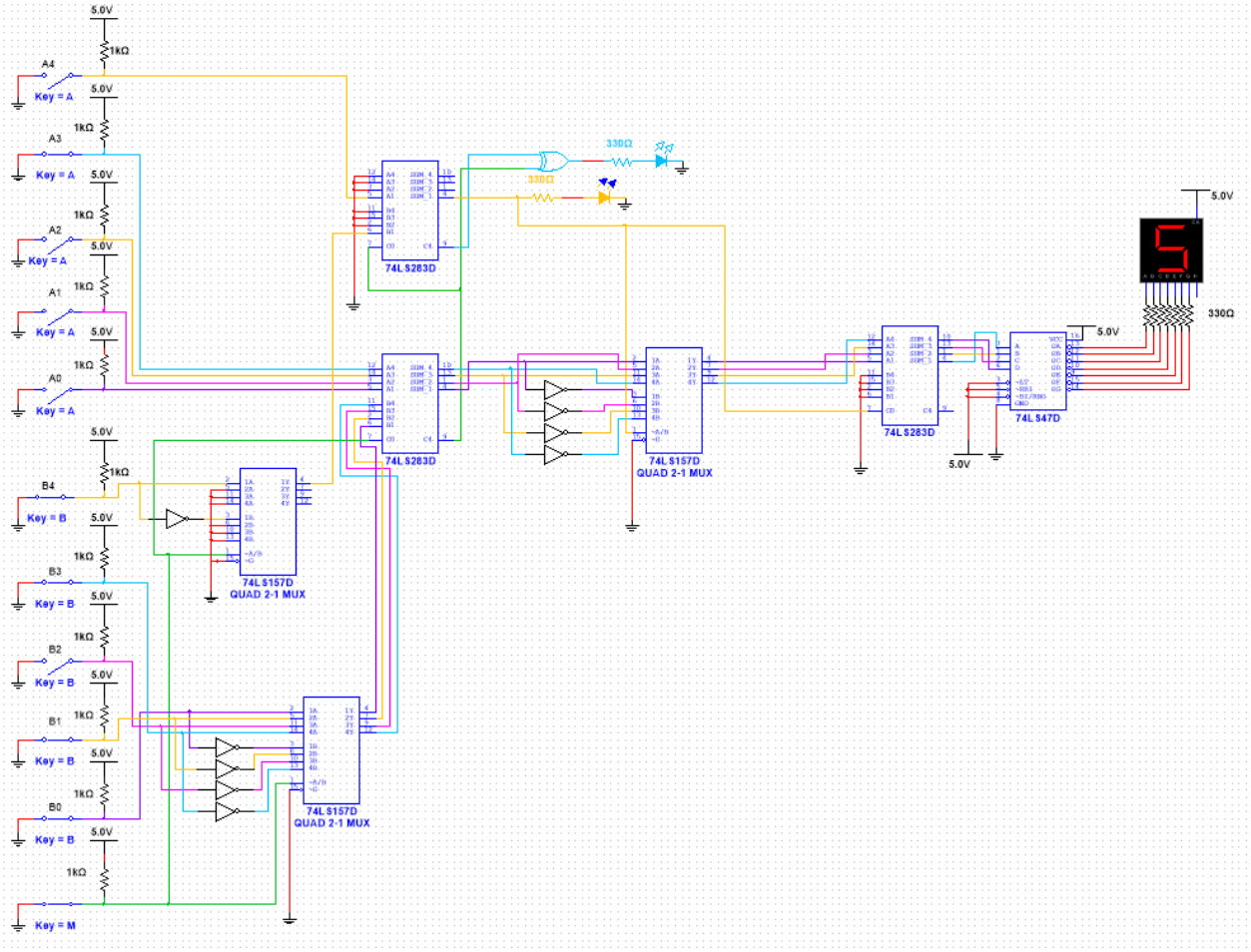
Figure 0.1 : Full Adder/Subtractor in 2's compliment



0.2 Design of a 5-bit Signed Adder-Subtractor Circuit Using Full Adders, Multiplexers, and Logic Gates with BCD Output and LED Indicators for Sign and Overflow

Figure 0.2 : Full Adder/Subtractor in 2's compliment using MUX

USING QUAD-2-1 MUX 74LS157D



1.0 **INTRODUCTION**

In this lab, we implemented a 5-bit adder/subtractor circuit using full adders, multiplexers, and display logic to show signed results on a seven-segment display. The design demonstrates two's complement arithmetic and overflow detection using standard TTL ICs.

2.0 **OBJECTIVES**

The goal is the following:

1. To design a 5-bit adder/subtractor using full adders and Exclusive-OR gates.
2. To display the signed result in BCD form on a seven-segment display.
3. To indicate the **sign** and **overflow** conditions using LEDs.
4. To verify that subtraction works correctly even when A < B.

3.0 **REQUIREMENT**

Implement the adder/subtractor circuit using SSI/MSI chips. The design must meet the following requirements:

1. Use **three 74LS283** (4-bit full adders) for arithmetic.
2. Use **three 74LS86** XOR gates to control input inversion for subtraction.
3. Use **one 74LS47** for seven-segment decoding.
4. Use **one seven-segment display** for output.
5. Use **two LEDs** for sign and overflow indication.
6. Verify both addition and subtraction operations for all valid input combinations.

4.0 **PARTS LIST**

The Parts list for this experiment is shown below in Table 4.1

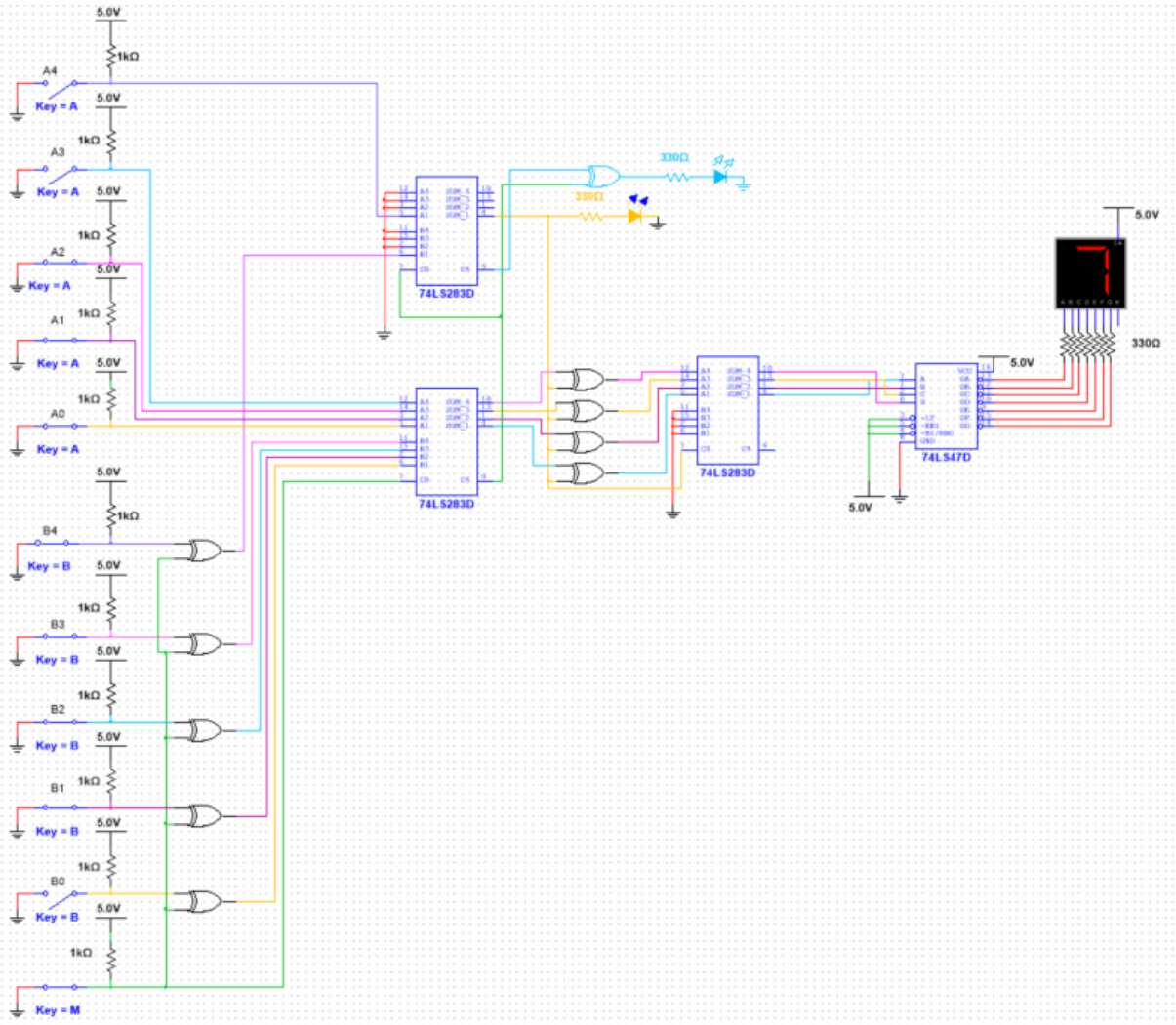
Table 4.1 - Parts List

Item No.	Part Number	Function	Quantity
1	74LS283	4-bit Full Adder	3
2	74LS86	XOR Gate	3
4	74LS47	BCD-to-7-Seg	1
5	7-Segment	Output	1
6	DIP Switch	Input	2
7	LED	Output	2

5.0 **DESIGN/IMPLEMENTATION**

The adder/subtractor was implemented using cascaded 74LS283 full adders.
The XOR gates (74LS86) invert the B inputs when M=1 (subtraction).
The sign bit is taken from the MSB of the result, while overflow is detected from the carry-in and carry-out of the MSB adder stage.

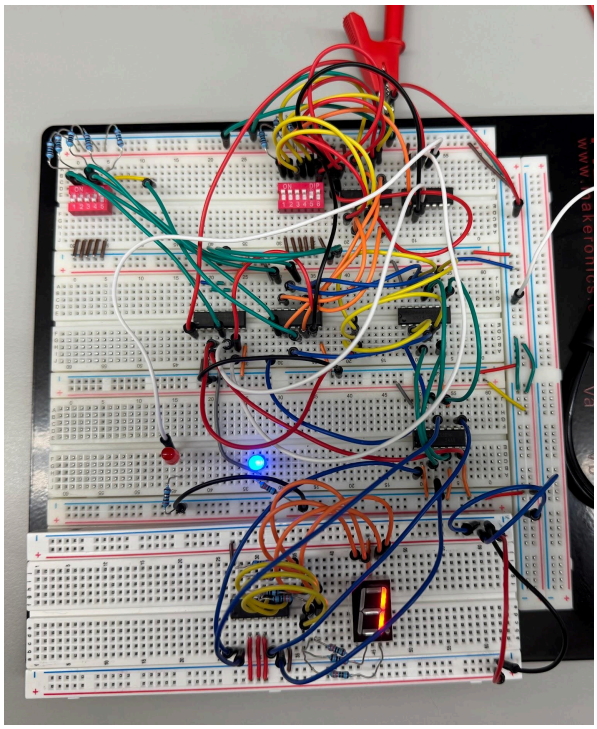
The resulting binary output is converted to BCD and displayed using a 74LS47 driver and a seven-segment display. LEDs indicate negative results and overflow conditions.

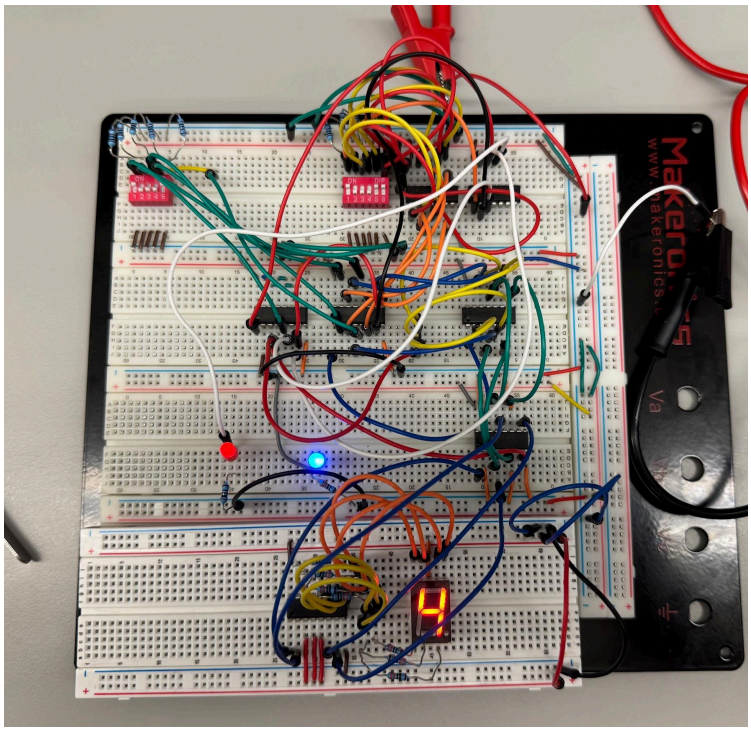


6.0 **TEST SETUP**

The circuit was constructed on a breadboard using DIP switches to input A_4–A_0, B_4–B_0, and mode select M.
Outputs were connected to the seven-segment display through the 74LS47 and to LEDs for sign and overflow.

For testing, all combinations of A and B were tested for both M=0 (addition) and M=1 (subtraction). Observations of the seven-segment display, sign LED, and overflow LED were recorded.





7.0 **TEST RESULTS/VERIFICATION MATRIX**

Examples of the test results are summarized below in Table 7.1:

Table 7.1 - Truth Table of Circuit

A (5-bit)	B (5-bit)	M	Operation	Result (Binary)	Result (BCD)	Sign LED	Overflow LED
00001 (+1)	00111 (+7)	0	A + B	01000	8	Off	Off
11000 (-8)	00011 (+3)	0	-A + B	11011	5	ON	Off
01101 (+13)	11111(-1)	0	A + (-B)	01100	12	Off	Off
10011 (−13)	11010 (−6)	0	-A + (-B)	01101	13	Off	ON
01111 (+15)	00100 (+4)	1	A - B	01011	11	Off	Off
10100 (−12)	00001 (1)	1	-A - B	10011	13	ON	Off
01000 (+8)	11110 (−2)	1	A - (-B)	01010	10	Off	Off
11111	10111	1	-A - (-B)	01000	8	Off	Off

8.0 Conclusion

The 5-bit adder/subtractor circuit was successfully designed and tested.
The use of XOR gates correctly implemented two's complement arithmetic.
Both sign and overflow detection operated as expected, and results were accurately displayed on the seven-segment display in BCD form.
The design verified that subtraction works properly even when A < B, demonstrating correct handling of negative values.

9.0 Post Lab

Design a combinational circuit that performs the following function:

S1	S0	Y
0	0	0
0	1	A
1	0	B
1	1	$(15)_{10}$

Assume A is a 4-bit number and B = $y_3'y_2'y_1'y_0'$. Draw a logic diagram implementing this circuit.

The simplified Diagram 9.0 below shows the above functions. When both selects are 0, Y=0, or Gnd. When only S0 is 1, Y is the A input. When only 1 is 1, Y is the B inputs.And finally, when both selects are 1, Y=15, or Vcc.

Diagram 9.0